design of Synchronous Controller to Minimize Response time and Power (type Research)	
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Encadrant(s) : Bouraoui ouni	
Description: As power dissipation and time constraint have become vital challenges during the creation of a digital circuit, researchers and designers efforts have increased to figure out new ways of preserving power through the study of its sources and its impacts as well as through the decrease of response time to obtain faster circuits. However, it is widely acknowledged that these two parameters are antagonistic in synchronous systems. In fact the current technologies have only managed to further decrease the response time to have a faster circuit at the cost of a considerable simultaneous augmentation in its power or vice versa which leaves no option for designers but to choose from these two important parameters. Hence, our main objective is to develop a design method that simultaneously builds a low power design and provides a faster circuit. For the achievement of that purpose, we have chosen a controller based on a finite state machine (FSM) as an example of synchronous system to prove that our design can optimize both parameters: time and power.	[1] Choudhury, Priyanka, Pradhan, Sambhu Nath "An Approach for Low Power Design of Power Gated Finite State Machines Considering Partitioning and State Encoding Together" Journal of Low Power Electronics, Volume 8, Number 4, August 2012, pp. 452-463(12) [2] Jason Cong, Wei Jiang, Bin Liu, Yi Zou, "Automatic memory partitioning and scheduling for throughput and power optimization", Computer-Aided Design - Digest of Technical Papers, 2009. ICCAD 2009. IEEE/ACM International Conference on 2-5 Nov. 2009
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