Hardware Software Partitioning of Control Data Flow Graph on System On Programmable Chip (type Research)	
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Description: A System On Programmable Chip (SOPC) is a circuit that integrates all components of an electronic system into a single chip. It may consist on memories, one or more microprocessors, interface devices, configurable logic blocs and other necessary components to achieve the intended function. In this work we aim to propose a new hardware-software partitioning algorithm of control data flow graph for SOPC. The main aim the algorithm is to find a best trade-offs between hardware and software implementation of operations in order to satisfy design constraints in term of latency and hardware resources of the target application	[1] S. Banerjee, E. Bozorgzadeh, and N. D. Dutt, ''Integrating physical constraints in hw-sw partitioning for architectures with partial dynamic reconfiguration, '' IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 14, no. 11, pp. 1189 –1202, nov. 2006.) [2] J. Wu and T. Srikanthan, ''Low-complex dynamic programming algorithm for hardware/software partitioning,'' Information processing letters, vol. 98, no. 2, pp. 41–46, 2006.
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